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|  devices & electronics:COURSE PROJECT |
| Digital to Analog Converter |
| Using MOS current sources, current switches and W, 2W Mosfet Ladder Network (4-bit implementation) |
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| **12/12/2011** |

# Objective:

We designed a Digital to Analog Converter, with a 4 bit design which can be extended for the 8 bit implementation. The design and implementation of the device is given here.

# Design:

There are five basic implementations of a DAC. The basic needs of the design are,

Components we need,

• Reference

• May be either Voltage or Current

• Reference Divider (Voltage or Current, Time)

• May be Resistor, Capacitor, or Transistor based

 • Switches and, or combiner

1. One is the Voltage mode and Binary Weighted Resistors (R, 2R, 4R, 8R in parallel).
2. Second is the Voltage mode and R, 2R Ladder Network.



1. Third is Current Mode with Binary Weighted Resistors.
2. Fourth is the Current Mode and R, 2R Network.
3. Fifth one is the Current Mode and W, 2W MOS transistors only Network.

**We used the fifth one**; **Current Mode with the W, 2W Ladder Network**. There are two reasons for that,

1. We are not using the voltage mode as it is not an industrially desirable design. A lot of transistors can be assembled in a small chip; the resistors take a lot of space.
2. Selection of the W, 2W network is advantageous because it is easy to assemble, especially if we want an 8 bit or higher resolution DAC implementation. We can easily see that in this configuration, we have



1. We use this implementation because it uses no resistors (only the feedback resistor for acquiring the output). Moreover because of the parallel and series combinations of the MOS transistors, one can implement using the R, 2R analogy

 

This is one of the advantages of this implementation.





# \*\* In the figure above the transistors used are NMOS.

\*\*\* In the last M6 transistor, the drain is connected to the 5 volts permanently. Because this is the second branch where the “Iref/8’s” second part is passing (Iref/16)

# Implementation:

In the Current Mode design we will have a W, 2W ladder network current divider. At each node we have binary multiple of the current before that node. These are the “binary weighted” currents, which depend on the BINARY INPUT we give to the CURRENT SWITCHES. These currents add up (the magnitude depends upon the Vref (Iref) and the binary input we give to the current switches. We will implement using following:-

1. We have to have theoretically identical current sources, which we will implement using MOS transistors. One implementation is simple, that is to use each transistor biased in saturation region. We can use a more robust design by biasing one transistor for a specific current and use its Vds to manipulate the gate voltage of the other transistor. This other transistor will drive a specific current at each node.
2. The **switches** which we see in the diagrams are basically the current switches, which will also be implemented with the help of MOS transistors. We will control the voltage at the gate of one of the transistors which determine the direction of current flow. Following figure represents the NMOS implementation of a switch and a simple current source.

**We did not use manual switches. Of course if user wants to use this device somewhere in his/her circuit for some purpose, there must be internal digital transistor based switches with can turn on/off with the help of digital input. The NOISE MARGINS, VOL, VOH, PROPAGATION DELAY OF THE INVERTORS USED, ETC. are given on the page after next page.**



\*\* The above figure is just one of the four switches.

\*\* The amplifier is not the part of the switches; it is just showing the output stage. Current from all the binary coded sources pass towards the –ve terminal of the op-amp. The negative feedback resistor gives the relation between output and the current Vo = IRref

 **Switches** were implemented as follows,

1. **Inverters**:

Inverters were implemented using the NMOS, PMOS pairs of the CD4007 IC. We used 2 ICs because there were four switches to be made. The basic diagram of the implementation with the propagation delay etc. of one of the inverters tabulation is also given below.



1. The transistors M1 and M2 used in the switching purpose are not CD4007 IC Mosfets, they are 2N7000’s which can support higher currents without posing any problem.
2. We will use an Op-Amp afterwards. All the currents will go to the virtual ground of the op-amp which is being used with a feedback resistor Rf. The output will be the desired analog voltage, scaled to the desired resolution.
3. Once we have the basic characteristics of this configuration understood, we can easily formulate biasing and the circuit configuration for the MOS. If we analyze our circuit, we can easily show that the currents are indeed binary coded.

# Design Considerations and Bias Calculations:

1. **Mismatch Problem**:

As we know that the aspect ratio, Capacitance and other trans-conduction parameters of the MOSFETs are different for the MOSFETs in different ICs and sometimes this happens for the same IC MOSFETS as well. So due to this mismatch our current sources will not be exact that will affect our resolution. So for our project first of all we collected the ICs of the same company. Then we used simple experimentation to further get those with same parameter “k”. This way we minimized the mismatch problem.

1. **Body Effect**:

When the sources and body are not at the same potential, there is body effect. So to minimize this effect we used only one MOSFET of the three in the CD4007 IC. So, for the Main Network we used 12 CD4007 ICs.

1. The transistors M1 and M2 used in the switching purpose are not CD4007 IC Mosfets, they are **2N7000’s** which can support higher currents without posing any problem.
2. We have not taken into account the **pinching off effect** while biasing the current mirrors, etc. as the ***channel-length modulation parameter (*λ)** in our calculations of biasing λ = 0.014 (VA = 80V).

**Calculations:**



1. **Biasing:**

We biased the Iref/2 to be 0.8 mA. Rd was calculated as follows.

As the Drain is connected to the Gate, Vgs = Vds. KN = 0.5, Vt = 1.3.

So,

 Vds = sqrt(2\*Iref/2\*1/kn) + Vt

 = 3.08 V

 Rd = (Vdd – Vds)/I = (10 – 3.08)/0.8 = 8.65 kOhms

We used 8.2k in combination with the 520 ohm resistor.

1. **Calculation of the Rref:**

Let us start with all the switches on. When all switches will be on, double the Iref/2, meaning 1.6 mA will flow through the Rref. And we should get approximately 10 Volts at the output. So,

 V = IRref

 Rref  = 10/1.6 = 6.25 kOhms

For other values of the inputs (the other 15 binary combinations), the voltage will change, current being scaled to output by Rref, AND THE SMALLEST INCREMENT BEING Vmax/16, which in our case will be 10/16 = 0.625 V.

**Measurements:**

1. **Settling time:**

Setting is time for converter to settle to within a specified resolution (typically 0.5 LSB). As measured from the oscilloscope, the average settling time was approx. **100ns.**

1. **Sampling rate:**

It is typically inverse of the settling time.

Sampling rate = 1/settling time = 1/100ns = 1x10^-7 = 10 MHz

# Uses of this Device:

Used at the end of a digital processing chain where analog signals are required.

• Digital Audio

– CD / MP3 Players, HD radio, Digital telephones

• Digital Video

– DVD Players, DTV, Computer displays

• Industrial Control Systems

– Motor control, valves, transducer excitation

• Waveform Function Generators, test equipment

• Calibration / tuning in embedded systems, built-in self test

# Terminologies and the Equations:

1. **Binary word:**



We call it the input binary word, where b1 is the most significant and bN is least significant. This can also be called a Digital Signal which determines the resolution of the DAC and is the basic input method to get required analog output.

The output current will be,

I0 = D\*Vref/Rf

Vout= Vref*b*1\*2-1+ *b*2\*2-2 + + *b*n\*2-n

This is basically sum of all the “binary weighted currents” controlled by the binary input through current switches.

1. **D/A Settling Time and Sampling Rate:**

• Settling time — time for converter to settle to within a specified

 resolution (typically 0.5 LSB)

• Sampling rate — max rate (typically inverse of settling time)